EXTENDED DATASHEET

MCA527NANO / NANO+

DESCRIPTION

The MCA527nano is a very small ultra-low power multichannel analyzer module designed for direct integration into a detector housing. It is intended for use in NaI- and CdZnTe-detectors but it is also suitable for other applications such as neutron counters or CsI detectors. In conjunction with a preamplifier and a high voltage power supply it is possible to realize an ultra-compact spectrometer. Thanks to its very small footprint, it is predestinated for usage in detector arrays. The MCA527nano+ can operate with up to 16k channel resolution for HPGe detector purposes.

The module needs three different supply voltages for operation (2.5V, 1.8V, 1.0V / 1.2V). A logic level UART with up to 6.25MBaud transfer rate is available for communication with a host. It makes it easy to connect the module to various serial interfaces like RS232, RS485, USB or logic level UART. Four digital I/Os are available to extend the module's functionality. The pins GPIO1, GPIO2 and GPIO3 may be used as general-purpose input or output, counter, pulser or trigger input. Pulse gating functionality is available when using the GATE pin as gate input. The GPIO3 pin may be used to start a measurement synchronously to an external trigger event with a latency ≤100ns.

Because the MCA527nano is derived from the MCA527, it is fully firmware compatible with it. All existing application programs and programming libraries for the MCA527 product family can be used to operate the MCA527nano. The basic functions will always work well but for complete device support only the latest software versions should be used. Please check our website for newest software versions and documents.

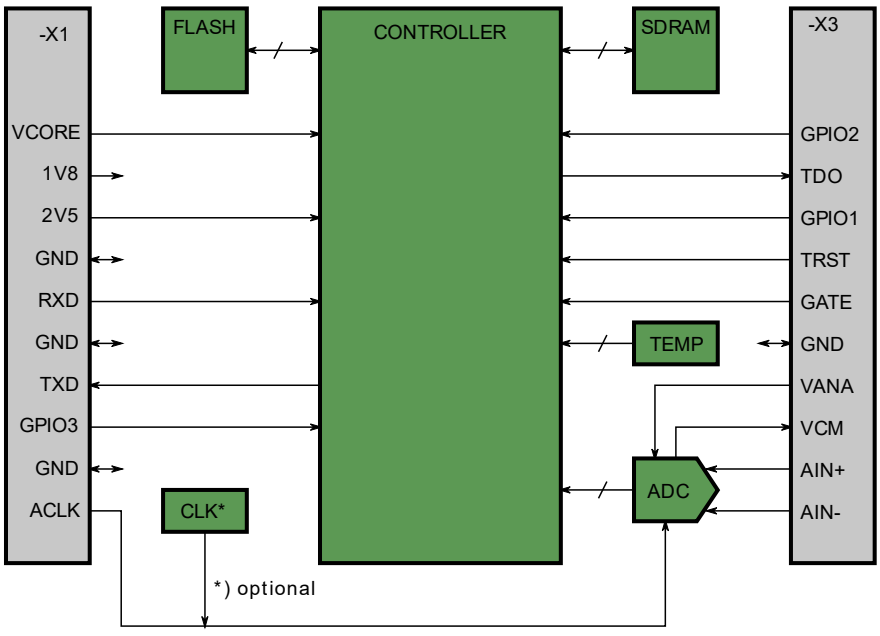

Figure 1 MCA527nano Block Diagram

Table 1 Absolute Maximum Ratings

Parameter	Rating
Supply Voltages V_{CORE} V_{ANA} V_{1V8} V_{2V5}	 -0.3V to +1.26V -0.3V to +2.0V -0.3V to +2.0V -0.5V to +3.0V
Digital Input Voltage (RxD, GPIO1, GPIO2, GPIO3, GATE, TRST, ACLK)	-0.3V to (V_{1V8} +0.2V)
Analog Input Voltage (AIN+, AIN-)	-0.3V to (V_{ANA} +0.2V)
Operating Temperature Range	-40°C to +70°C
Storage Temperature Range	-40°C to +125°C

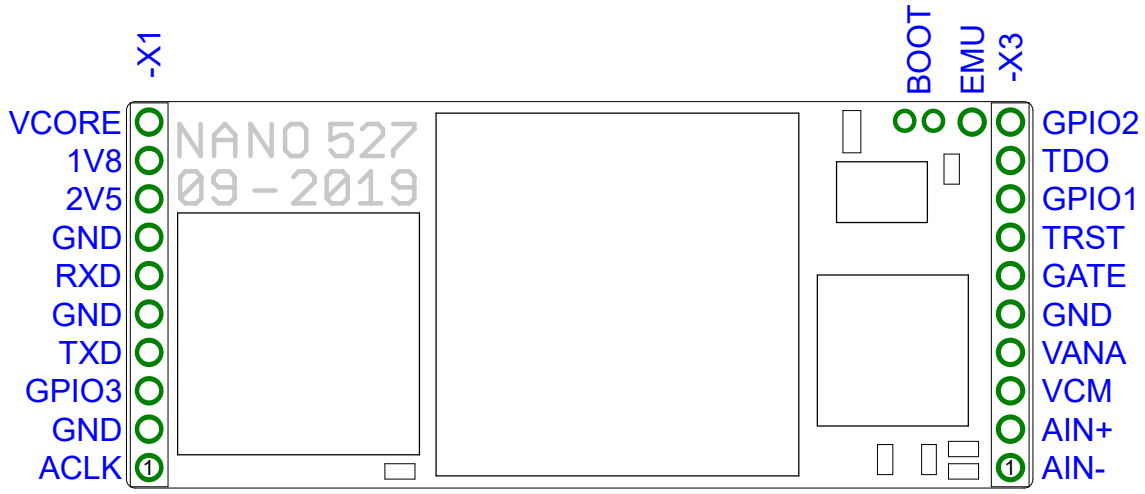

Figure 2 Connection Diagram (Top View)

Table 2 -X1 Pinout Description

Name	Pin	Type	Description
VCORE	10	Supply	**Core Supply Voltage:** Supply voltage for the controller's core.
1V8	9	Supply	**1.8V Supply Voltage:** 1.8V supply voltage for the module.
2V5	8	Supply	**2.5V Supply Voltage:** 2.5V supply voltage for the controller.
GND	2, 5, 7	Supply	**Ground:** Ground supply pins.
RXD	6	In	**UART Receiver:** Data input of the controller's host UART.
TXD	4	Out	**UART Transmitter:** Data output of the controller's host UART.
GPIO3	3	I/O	**GPIO3:** This pin may be used as general-purpose input / output or as counter 3 / pulser 3. Furthermore, it could be used as trigger input (latency up to some µs) or as fast trigger input (latency ≤100ns). It is pulled down with 10 kΩ.
ACLK	1	In	**Analog Clock:** Sample clock for the ADC

Table 3 -X3 Pinout Description

Name	Pin	Type	Description
AIN-	1	In	**Negative Differential Analog Input:** The output of the ADC driver (preamplifier) must be connected to AIN+ and AIN-. The signal should swing ±0.5V around the common mode voltage VCM (0.9V). In a single-ended configuration this pin should be driven at 0.9V.
AIN+	2	In	**Positive Differential Analog Input:** The output of the ADC driver (preamplifier) must be connected to AIN+ and AIN-. The signal should swing ±0.5V around the common mode voltage VCM (0.9V). In a single-ended configuration this pin should swing ±1.0V around AIN- (0.9V).
VCM	3	Out	**Common Mode Bias:** A 0.9V reference voltage is supplied to the ADC driver (preamplifier) on this pin. It can be used to bias the preamplifier.
VANA	4	In	**Analog Supply Voltage:** Dedicated supply voltage for the ADC (1.8V). For best analog performance, this voltage must be free of any noise.
GND	5	Supply	**Ground:** Ground supply pins.
GATE	6	I/O	**Gating:** This pin may be used as gating input. In JTAG mode it is used as TMS (JTAG Mode Select). It is pulled down with 10 kΩ.
TRST	7	In	**JTAG Reset:** This digital input is only used in JTAG mode (TRST). It is pulled down with 10 kΩ.
GPIO1	8	I/O	**GPIO1:** This pin may be used as general-purpose input / output or as counter 1 / pulser 1. Furthermore, it could be used as trigger input to start a measurement (latency up to some µs). In JTAG mode it is used as TCK (JTAG clock). It is pulled down with 10 kΩ.
TDO	9	Out	**JTAG TDO:** This digital output is only used in JTAG mode (JTAG serial data out).
GPIO2	10	I/O	**GPIO2:** This pin may be used as general-purpose input / output or as counter 2 / pulser 2. Furthermore, it could be used as trigger input to start a measurement (latency up to some µs). In JTAG mode it is used as TDI (JTAG serial data in). It is pulled down with 10 kΩ.

Table 4 Other Pins

Name	Pin	Type	Description
BOOT			**Boot Mode Control:** For normal operation both pads should be unconnected. When the pads are shorted during power-up, the controller boots into a special rescue mode for firmware programming.
EMU		Out	**Emulation/Test Control:** JTAG Emulation Output

Table 5 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
V_{CORE}	Core Supply Voltage		0.95 [1]		1.26	V
V_{ANA}	Analog Supply Voltage		1.7		1.9	V
V_{1V8}	1.8V Supply Voltage		1.7		1.9	V
V_{2V5}	2.5V Supply Voltage		2.25		2.75	V
I_{CORE}	Core Supply Current [4]	Idle [2] Measurement [2] [3]		50/65/85 100/130/170		mA
I_{ANA}	Analog Supply Current	Idle [2] Measurement [2] [3]		24 24		mA
I_{1V8}	1.8V Supply Current	Idle [2] Measurement [2] [3]		17 18		mA
I_{2V5}	2.5V Supply Current	Idle [2] Measurement [2] [3]		0.1 0.1		mA
P_{tot}	Total Power Consumption [4]	Idle [2] Measurement [2] [3]		125/140/160 175/210/250		mW
Digital Inputs and Outputs						
V_{IH}	High Level Input Voltage	V_{1V8} = 1.9V	1.10			V
V_{IL}	Low Level Input Voltage	V_{1V8} = 1.7V			0.60	V
V_{OH}	High Level Output Voltage	I_{OH} = -0.5mA	1.35			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA			0.40	V
I_{IH}	High Level Input Current	V_{IN} = 3.6V			100	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V			10	µA
C_{IN}	Input Capacitance	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C		5	25	pF
ADC Characteristics						
V_{IN}	Analog Input Span			2		V_{PP}
V_{INCM}	Analog Input Common Mode Voltage Range		0.5	0.9	1.3	V
C_{INA}	Analog Input Capacitance			6		pF
	ADC Resolution		14			bit
f_S	Sample Rate		5	10	20	MSps
Dynamic Characteristics						
BR	UART Baud Rate		110		6.25M	Baud
t_{GATEON}	GATE Pulse Width		500			ns

[1] for processor speeds up to 400MHz, 1.14V for higher speeds
[2] all outputs unloaded
[3] input count rate 50kcps
[4] V_{CORE} = 1.0V, 400MHz / V_{CORE} = 1.2V, 400MHz / V_{CORE} = 1.2V, 600MHz

Power Supply

For proper operation, all four supply voltages V_{CORE}, V_{ANA}, V_{1V8} and V_{2V5} must be always within its specified limits. The V_{1V8} supply is monitored by an internal reset generator. If this voltage is below its minimum limit, the controller is hold in reset. Because the other supply voltages are not monitored, it must be ensured that they are within its specified limits not later than 10ms after V_{1V8}.

The analog supply voltage V_{ANA} is used to power the ADC. The internal reference voltage is derived from this supply. Therefore, the quality of this supply voltage has a direct impact on the analog performance of the MCA. It must be free of any noise, even LF noise. The usage of a low noise linear regulator is recommended. Using the V_{1V8} supply to power V_{ANA} will degrade analog performance in most cases because the digital components of the device are generating LF noise. However, if limited performance is acceptable and a simple system design is preferred, this may be an option.

Analog Frontend

The analog frontend consists of the two inputs AIN+ and AIN- and the analog output voltage VCM. Both inputs are connected directly to the ADC which has a differential input stage. It is possible to drive the ADC with a differential or a single-ended amplifier. Referred to the ADC, SNR and DNL are the same for both versions but INL and harmonic distortion of the single-ended version are degraded. However, in most situations the single-ended driver should work well. Both versions must be configured that the signals baseline is at about 10% of full scale for positive input signals and at 90% of full scale for negative input signals.

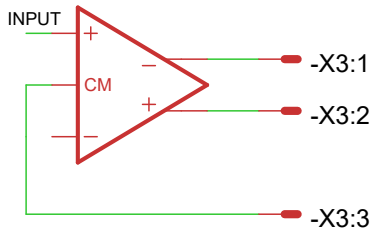

Figure 3 Differential ADC Driver

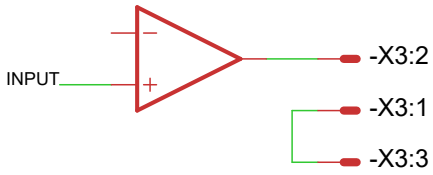

Figure 4 Single Ended Driver

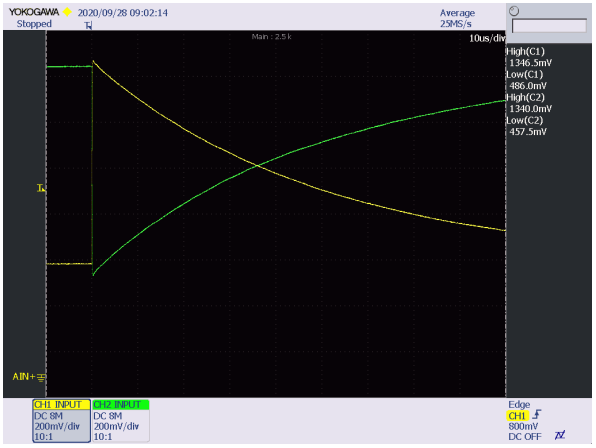

Figure 5 Signals of Differential Driver, V_{AIN+}=yellow, V_{AIN-}=green, V_{CM}=0.9V

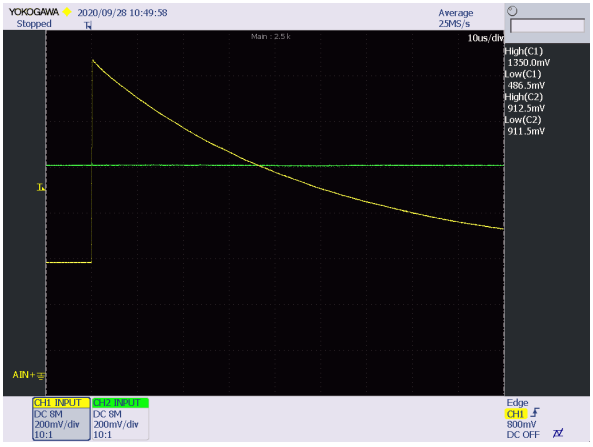

Figure 6 Signals of Single Ended ADC, V_{AIN+}=yellow, V_{AIN-}=green, V_{CM}=V_{AIN-}=0.9V

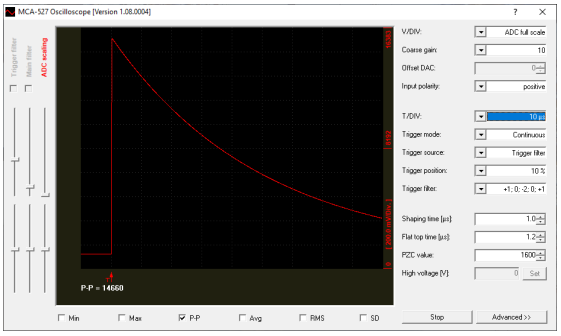

Figure 7 ADC Output for Figure 5 Signals

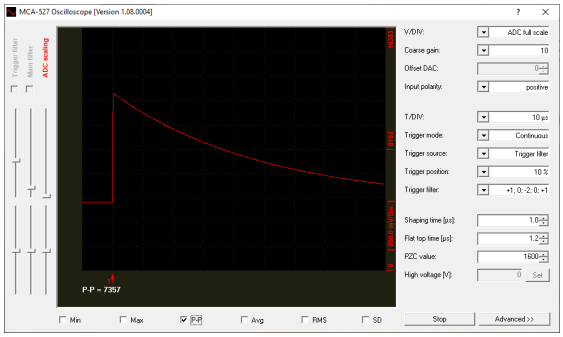

Figure 8 ADC Output for Figure 6 Signals

Figure 3 shows a differential driver stage. The signals AIN+ and AIN- must swing around the analog input common mode voltage (0.9V typical, Figure 5). VCM may be used to bias the common mode input of the ADC driver. When the previous stage has a single-ended output, the differential driver may be configured as single-ended to differential voltage converter.

A single-ended driver stage has two main advantages: It saves power and board space in most situations. Especially when a photomultiplier is used, only one operational amplifier is needed for pulse forming and ADC driving. Moreover, no additional noise is added to the signal by further operational amplifiers. In a single-ended configuration the signal AIN- should be driven with 0.9V, VCM may be used in most cases. The ADC range is limited to 90% in single-ended mode (A_{IN+}=0V … 1.8V, ADC full scale range = 2V).

The ADC output of Figure 8 gives a peak at about 95% of the spectrums full scale when the fine gain is set to 1 (same for Figure 7 at fine gain 0.5).

For best noise performance the bandwidth of the input signal must not be higher than 5MHz. It is recommended to use a low-pass filter directly before the ADC. The filters corner frequency should be set to 3.3MHz, higher values will only increase the noise. The higher the filters attenuation for high frequencies, the lower the noise seen by the ADC.

Host Communication

Communication with a host is possible by using the host UART. Currently five different baud rates are supported (38.4k, 115.2k, 307.2k, 3125k, 6250k). The baud rate is usually adjusted automatically but may be set manually, if required. The UART interface can be used directly by a microcontroller using its TTL signal lines or through an additional transceiver for various standard serial interfaces like USB, RS232 or RS485.

Boot Input

During power-up the controller of the MCA527nano checks the state of the BOOT pins. When they are left open, the controller tries to start the standard firmware. After booting the state of this pins is meaningless. However, if for any reason the firmware does not start, it is possible to bring the controller in a special rescue mode where only firmware programming is possible. For that, the BOOT pins must be shorted during power-up. With the GBS Firmware Loader a new firmware may be loaded to the flash of the MCA527nano through the host interface.

Gate Input

Just like the MCA527, the MCA527nano has also a gate input. It is accessible at the GATE pin of -X3. The following features for gated measurements of the MCA527 are available for the MCA527nano:

- turning gating on or off
- changing the gate signal polarity for gating by state in sort mode
- gating by time is available on MCA527nano+ version
- delay time adjustment

In sort mode, gated events are counted in a second spectrum. Sort mode is an option if doing stabilization with a LED-pulse on a NaI detector.

GPIO3 as Fast Trigger Input

This pin (-X1:3) may be used as trigger input to start a measurement synchronously to an external event with a latency of ≤100ns. The polarity can be changed by software.

Sample Clock

The MCA527nano is available with or without integrated sample clock generator. The version with integrated sample clock generator is intended for applications that uses only one MCA527nano while the version without clock generator is predestinated for applications with multiple MCA527nano.

The integrated sample clock generator runs at a constant frequency of 40MHz. This clock is divided by 2 or 4 within the ADC (controlled by software) to achieve an analog sample clock of 20MHz or 10MHz. If the integrated clock generator is used, the pin ACLK (-X1:1) has no function.

If an external clock source should be used for sampling, the MCA527nano must be ordered without sample clock generator. In this case the pin ACLK is used as sample clock input. Maximum allowed input frequency is 80MHz. For best performance, the duty cycle should be 50% ±5%. It is strongly recommended to use a low jitter clock source. The input clock is divided by 1, 2 or 4 within the ADC (controlled by software) to achieve the analog sample clock. Care must be taken to the ADCs maximum sample rate of 20MHz when selecting input clock frequency and clock divider.

Module Specification

Table 6 Module Specification

Parameter	Value
Host Interface	UART, 38.4kBd, 115.2kBd, 307.2kBd, 3125kBd, 6250kBd
Power Supply	2.5V, 1.8V, 1.0V / 1.2V
Typical Power Consumption (Idle / Measurement)	125mW / 175mW @ 400MHz 160mW / 250mW @ 600MHz
ADC	≤20MSps, 14bit, ≤0.02% INL, ≤0.01% DNL
Number of Channels	128, 256, 512, 1024, 2048, 4096[1],8192[1], 16384[1]
Shaping Time	0.1µs to 2µs (0.1µs to 25.5µs) [1], step 0.1µs
Flat Top Time	0µs to 15µs, step 0.1µs
Fine Gain Adjustment	0.5 to 6.5, step 0.0001
Trigger Threshold Adjustment	automatically / manually
Trigger Filter	Double and single [1] differential filtering
Pulse Pair Resolution	~400ns
Pile Up Rejection	yes
Throughput (0.2µs shaping time)	>100,000cps
Base Line Restorer	BLR with fixed/adjustable [1] averaging
Pole Zero Adjustment	Decay time down to 40µs can be compensated
Peak Stabilization Modes	standard mode, LED mode
Operation Modes	- PHA (Pulse Height Analysis) - MCS (Multichannel Scaling) - Sample Mode (Transient Record) - Oscilloscope Mode - Firmware Repeat Mode - Gating Mode (by state, by time[1]) - List Modes [2]
Special Features	- Integrated Temperature Sensor - various digital interfaces (UART, GPIO)
Operation Temperature Range	-40°C – 70°C
Dimensions	30mm x 12.8mm x 3.8mm
Weight	~2g

[1] Only available on MCA527nano+ version
[2] Optional available (option -LM)

Outline Dimensions of MCA527nano

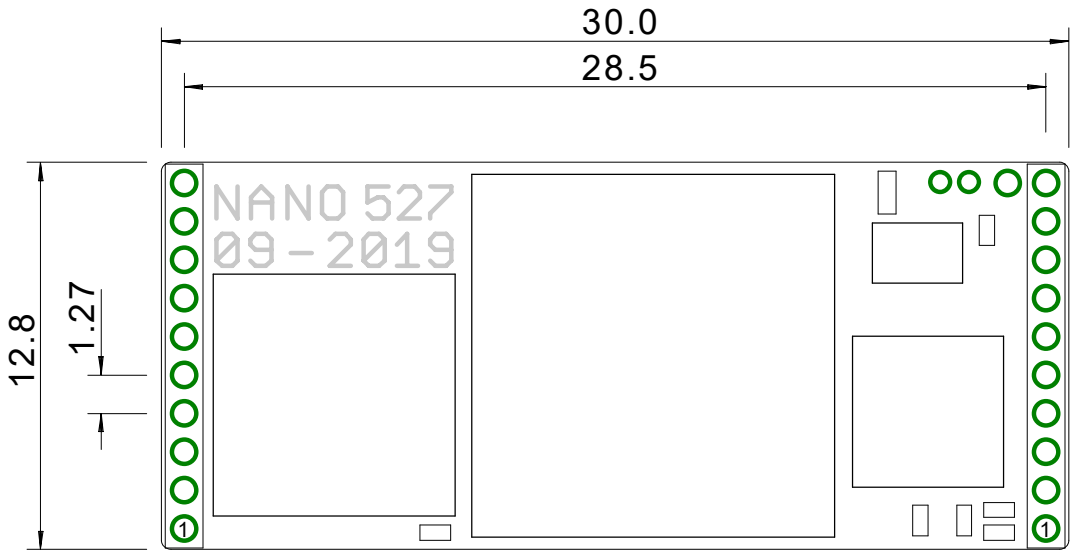

Figure 9 Outline Dimensions (Top View, all Dimensions are in Millimeters)

Order Codes

Order code	Description
A-GBS-MCA527NANO	Standard version with 4k resolution
A-GBS-MCA527NANO+	Extended version with 16k resolution
A-GBS-MCA527NANO-FW485	Standard version with 4k resolution and RS485 bootloader
A-GBS-MCA527NANO+-FW485	Extended version with 16k resolution and RS485 bootloader
A-GBS-MCA527NANO+-LM	Extended version with 16k resolution, list mode option
A-GBS-MCA527NANO+-FW485-LM	Extended version with 16k resolution and RS485 bootloader, list mode option

- Clock generator integrated or without
- Options generic?

Table 7 Revision History

Revision	Section / Figure / Entry	Correction
V21.01		Initial Version

Last update: 2021-01-20

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